

Exploring the Boundaries

Of Built in Test

Advances over the past 20 years in computing and compact memory technology have significantly improved the ability to incorporate sophisticated Built In Test (BIT) facilities into equipment.

This has enabled BIT to provide higher levels of confidence that the equipment will perform its intended functions, together with early warning of equipment failures and indications of probable failure locations. It has also reduced the equipment downtime otherwise caused by referring failures to external test resources, hence also reducing the need for these external test resources. Racal is at the forefront of these developments and is incorporating sophisticated BIT into its latest products.

The growing success of BIT technology has led to wide expectations that BIT can become so comprehensive as to eliminate the need for external test equipment altogether, apart from design qualification, manufacturing, calibration and base repair.

Alas, such aspirations tend to ignore the cost of perfecting BIT beyond current performance levels. They also overlook the fact that certain critical test functions are beyond the boundaries of BIT operation. Furthermore, they tend to ignore the additional cost and unreliability penalties of BIT functions and the challenge of building in tests of BIT itself.

BIT in Defence.

Racal has long recognised the particular significance of BIT in defence systems, where operational availability is a critical requirement. BIT can have a major impact on the large investments in field maintenance resources necessary to maintain high availability in mobile battlefield environments.

However, we are faced with a growing complexity of battlefield systems in which increasing numbers of sub-systems, often derived from different technologies and different manufacturers, are integrated into a single complex weapons platform. Clearly, operators of such systems not only need sophisticated BIT facilities to provide immediate warning and location of malfunctions, but also a system integration of these facilities into a composite display at the operator's console.

BIT Performance

BIT performance is mainly specified in terms of fault detection, fault location (to a single LRU), false alarms and diagnostic errors.

In practice, over the past decade, actual performance figures have rarely achieved the higher specifications. This is largely due to a combination of the costs to achieve further improvement and certain fundamental limitations of built-in test facilities.

BIT tolerances are also prone to being too tightly aligned with the design parameters of the equipment under test, hence giving rise to

respond, nor does it test equipment response at an external interface. In effect, there is no external closed loop test. Such shortcomings, in communications equipment, for example, deny performance testing of RF output, receiver sensitivity etc.

Much the same is true for internal links between equipment modules, and the main concern expressed by test design engineers relates to their ability to test board level interconnections. However, useful advances have recently been made in this area, in the form of a Module Test and Maintenance (MTM) bus structure for inter-module testing. This was pioneered under the aegis of IEEE 1194.4, in association with the standardisation of test port access and boundary scan techniques.

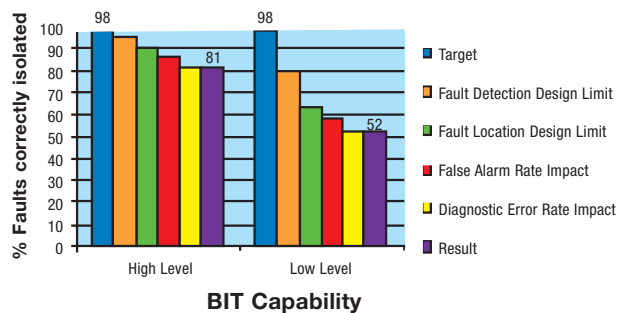
These techniques relate primarily to digital circuitry, and although A/D conversion is possible for analogue signature analysis this requires extra BIT circuitry and is difficult to achieve at high frequency sampling rates. The incorporation of additional BIT circuitry is also often inhibited by the limited number of access pins to the Unit Under Test (UUT).

Having attained the maximum amount of BIT circuitry, this still leaves the external, often most vulnerable, interfaces untested. It also introduces more hardware, and hence further unreliability into the equipment.

BIT Costs

By its very nature, the scope and performance of BIT is subject to the design constraints of the parent equipment, both functional and physical. The resultant design and cost penalties for a small improvement in BIT capability may well outweigh intended benefits. Effectively, improvement of BIT beyond the current performance figures may require a respective exponential increase in original design costs. Additionally, it must be remembered that BIT must be incorporated into every individual equipment, with consequent additions to cost

BIT Performance Factors



over-sensitivity or ambiguity in operational performance. Also, equipment architectures often do not suit the application of BIT, being insufficient in either physical or functional modularity.

Such factors may account for much of the continued high incidents of No Evidence Of Failure (NEOF) when items designated as failures by BIT are returned to either the manufacturer, or the in-service workshop for repair. It is an essential feature of Racal's design strategy to reduce such occurrences to the absolute minimum.

BIT Limitations

BIT's essential limitations lie in the fact that BIT is fundamentally an internal monitoring device. It does not provide the external stimuli to which the equipment is designed to

and unreliability.

It has been estimated that current test features in electronic design, including state-of-the-art BIT, account for over 25 per cent of product cost, an investment that must pay for itself over a product's service life. Cost implications must be similarly resolved when BIT is subsequently changed to accommodate in-service modifications.

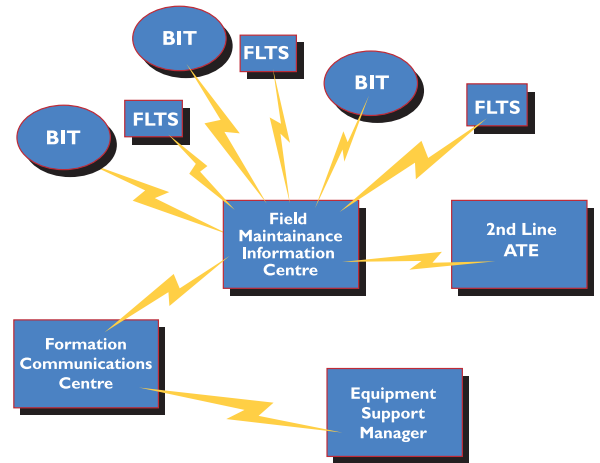
Test Strategy

In order to optimise the degree of BIT required, testability studies must first be undertaken to identify BIT designs capable of carrying out the various test and diagnostic functions, and to determine appropriate performance levels. These are then evaluated, within logistic support analysis (LSA) and life

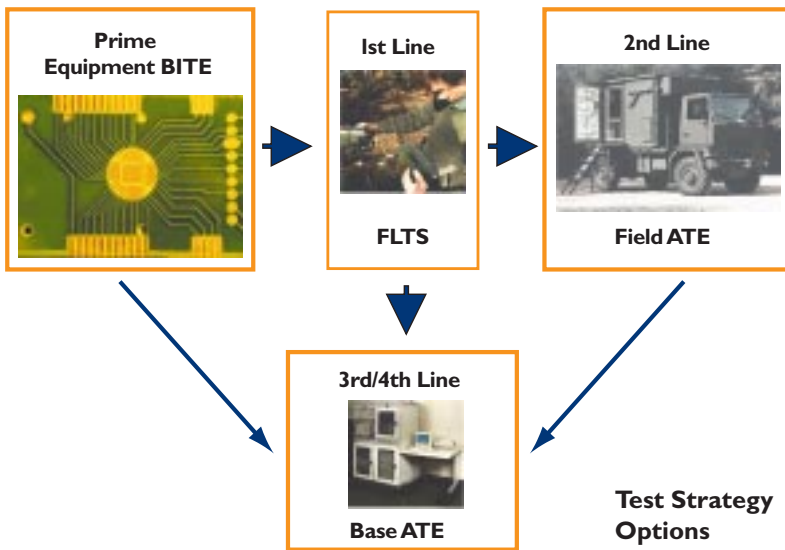
cycle costing (LCC) frameworks, against the alternatives of external test equipment (ETE) or living without certain test functions. Similar exercises can be applied to BIT/ETE as test-only and test-plus-diagnosis options.

ity, preferably when the design is sufficiently well established for an outline Failure Mode Effect and Criticality Analysis (FMECA) to be undertaken. The first and subsequent refined FMECAs form the basis of the testability study, which determines the test techniques and test interfaces required. The UUT design can then be examined to establish the potential for these requirements to be addressed by BIT.

At this stage the cost of BIT should be assessed against the ETE alternative, including the option of BIT fault detection coupled with ETE fault location.



Repair & Maintenance Data flow in Battlespace Digitization



cycle costing (LCC) frameworks, against the alternatives of external test equipment (ETE) or living without certain test functions. Similar exercises can be applied to BIT/ETE as test-only and test-plus-diagnosis options.

Most ETE addressing a UUT embodying some BIT will endeavour to exploit the BIT facility as a dynamic test interface. The ETE may be a First Line Test Set (FLTS) interfacing directly with the equipment in-situ, or a workshop test system interfacing with the LRU. The FLTS need not necessarily enhance the BIT, but provide an umbilical extension of the BIT system's processing and display functions. This in itself may reduce the space and reliability penalties of a wholly internal BIT system, while reducing the BIT investment through its ability to address more than one equipment.

The appropriate strategy is therefore to adopt a harmonised BIT plus ETE approach, in which BIT's technical and economic boundaries can be determined within an overall BIT/ETE framework.

Design Processes

To achieve effective and cost-efficient BIT, it is important that the design is integrated with that of the UUT at the earliest opportu-

Given this integrated approach, UUT and test resources can undergo parallel development, and expensive redesign at a later stage is eliminated. Effectively, test and testability requirements are treated as fundamentals of system design.

Battlespace Digitization

Digitization in defence operations presents new opportunities for systematic, large-scale field testing, and Racal is playing a major pioneering role in these. Within the framework of Battlefield Information System Applications (BISAs) it will be possible for BIT messages, together with data from the Health and Usage Monitoring System (HUMS), to be generated into the BISA. This would enable equipment status and condition to be assessed remotely by local maintenance support organisations, in addition to the operator's display. It will also be possible for the generation of such test information to be commanded through the BISA, by either scheduled or interceptive interrogation.

Such capabilities could have further cost and reliability implications, requiring careful cost benefit analysis prior to their introduction. However, the readily available spectrum of BIT information, representing experiences

of actual fault occurrences and remedies, across a comparative equipment population, could assist in devising measures for reliability growth, reliability-centred maintenance and improved fault diagnosis.

Conclusion

BIT already plays a vital role by maximising user confidence that an equipment is fit for operation. It performs an increasingly important role by enhancing the testability of complex equipment, particularly where miniaturisation constraints reduce access by external test equipment. It will have growing importance in the era of battlespace digitization, which offers opportunities for BIT data to be transmitted for remote analysis and prediction.

Nevertheless, against the benefits of BIT must be weighed the cost, limitations and drawbacks at the outset of an equipment's design strategy. The BIT potential must be properly evaluated with alternatives to ensure maximum life cycle cost-effectiveness. It is unlikely that BIT will ever stretch its essentially internal boundaries to eliminate totally the need for external test resources.

Racal assures optimised BIT performance coupled with the most cost-efficient supporting test solutions. This can only be realised by ensuring that through-life support considerations are taken into account during design, alongside prime equipment performance criteria. This demands early involvement of test requirements in the prime equipment design, and of parallel research for both BIT and external test options. The BIT display is often the first thing an operator sees when switching on his equipment. We must avoid customer disappointment by ensuring that BIT undertakes only those functions for which it is most suited.